IEEE International Defect Based Testing Workshop –DBT'07
October 25th – 26th, Santa Clara Convention Center, California

Day 1 – Thursday, October 25th

*4:00pm – Opening Remarks –**H. Manhaeve** (Q-Star Test), **M. Tehranipoor** (Univ. of Connecticut)*

4:10pm – 5:10 pm

***Thursday Keynote*:** Defect-Based Test: What is Our Data Telling Us?

Kenneth M. Butler (*Texas Instruments)*

*Session 1: Chair – **Sreejit Chakravarty** (LSI Logic)*

5:10pm – 6:30pm

30: We Are Done with Scan & Memory BIST. Where is DFT Headed Next? (*Invited Talk*)

R. Raina *(Freescale)*

30: Defect Based Testing / A Diagnostics Perspective (*Invited Talk*)

T. Bartenstein (*Cadence*)

20: High Speed Localization and Visualization of Blocked Chain Defects

J. Orbon & **A. Crouch** (*Inovys*)

Workshop Welcome Reception - 7:00pm – 9:00pm

Day 2 – Friday, October 26th

8:00am – 9:00 am

Friday Keynote: Opportunities with Process Variation

TM Mak (*Intel)*

*Session 2: Chair – **Xiaoqing Wen** (Kyushu Institute of Tech.)*

9:00am – 10:20am

20: Dynamic N-Detect Patterns Based on Equivalent Faults

P. Reuter and Y. Huang (*Mentor Graphics*)

15: Small Delay Defect Detection Using Self-Relative Timing Bounds

R. Helinski, J. Plusquellic (*UMBC*) and M. Tehranipoor (*Univ. of Connecticut*)

15: Interconnect Open Detection by Supply Current Testing under AC Electric Field Application

M. Hashizume, **Y. Ogata**, M. Tojo, M. Ichimiya, H. Yotsuyanagi (*Univ. of Tokushima*)

15: Temporal Analysis and Spatial Deconvolution of Power Pad Transients Signals for Fault Localization

R. M. Rad and J. Plusquellic (*UMBC*)

15: Towards an Optimal Combination of Logic and Current tests in Function of Product Quality and Test Cost Requirements

H. Manhaeve, S. Kerckenaere (*Q-Star Test*), G. Eide (*Magma*), J. Brenkuš (*Slovak Univ. Tech.*)

Coffee Break- 10:20am – 10:40am

*Session 3: Chair – **Anuja Sehgal** (AMD)*

10:40am – 12:00pm

20: Test-Pattern Grading for Small-Delay Defects

M. Yilmaz, K. Chakrabarty (*Duke University*), M. Tehranipoor (*Univ. of Connecticut*)

20: A Method for Improving the Bridging Defect Coverage of a Transition Delay Test Set

K. Miyase, X. Wen, S. Kajihara, M. Yamamoto, and H. Furukawa (*Kyushu Institute of Technology*)

20: Theoretical and Practical Aspects of IDDQ Measurement Settling

B. Straka, **H. Manhaeve** (*Q-Star Test*), J. Brenkuš (*Slovak Univ. of Tech.*), S. Kerckenaere (*Q-Star Test*)

20: On the Potential of Test Pattern Generation to Improve Current-Based Testing and Diagnosis Techniques

C. Thibeault (*Ecole de technologie supérieure*)

Lunch - 12:00 pm – 1:00pm

Session 4: Chair – ***Geir Eide*** *(Magma Design Automation)*
1:00pm – 2:20pm

30: Defect-Based Testing with Adaptive Flows (*Invited Talk*)

R. Daasch (Portland State University)

30: Defect & Failure Mode Trends (*Invited Talk*)

L. Chadwick and **P. Nigh** (*IBM*)

20: A Defect-Tolerant Interconnect Mechanism for Nanoscale Architectures

A. Namazi, **M. Nourani** and M. Saquib (*Univ. of Texas at Dallas*)

Short Break- 2:20pm – 2:40pm

2:40pm – 4:00 pm ***– Panel Discussion***
"Process Variations + Systematic Defects"

Organizers:

Hank Walker *(TexasA&M Univ.)*
Mohammad Tehranipoor *(Univ. of Connecticut)*

Panelists:

Rob Aitken *(ARM)*
John Carulli *(Texas Instruments)*
Al Crouch *(Inovys)*
Phil Nigh *(IBM)*