IEEE Int. Workshop on Defect and Data Driven Testing (D3T-2008)
October 30th – 31th, Santa Clara Convention Center, California

Day 1 - Thursday, October 30th
4:00pm - Opening Remarks: ***M. Tehranipoor*** *(Univ. of Connecticut)*

4:10pm - 5:00 pm
Thursday Keynote**:** Title: Technology Characterization for Successful Products
Dennis Ciplickas (*PDF Solutions*)

5:10pm - 6:50pm
Session 1: Defect-based Testing and Test Quality
Chair - ***Xiaoqing Wen*** *(Kyushu Institute of Technology)*

30: Generating High Quality Test Sets - how do we get there? (*Invited Talk*)
Nilanjan Mukherjee (*Mentor Graphics***)**
30: Title: 1149.1 Re-Use, P1687 and the future of JTAG-Based Data Collection *(Invited talk)*
Jason Doege (*AMD*)
20: The Economics of Defect-Based Testing
Chris Allsup (*Synopsys***)**
20: VDD-Ramp Test for Analog Circuits and Optimum Sampling Frequency Selection
M. Arabackyj, J. Ortner and W. Schirmer (*Universität Erlangen-Nürnberg***)**

Workshop Welcome Reception - 7:00pm - 9:00pm

Day 2 - Friday, October 31th

8:00am - 9:00 am
Tutorial: Green Eggs and Ham - An Outlier Elimination Tutorial. What should be thrown away? What should we keep?
Jeffrey L. Roehr (*MediaTek)*

9:00am - 10:20am
Session 2: Power-aware Test
Chair - ***Qiang Xu*** *(Chinese Univ. Of Hong Kong)*

20: GA-Based X-Filling for Reducing Launch Switching Activity in At-Speed Scan Testing
Yuta Yamato, Xiaoqing Wen, Kohei Miyase, Hiroshi Furukawa, and Seiji Kajihara (*Kyushu Institute of Technology*)
20: On a Dynamic Monitoring Approach for Power Noise
Claude Thibeault (*Ecole de technologie superieure*)
20: An Efficient Algorithm for Achieving Constant Test Power
Zhongwei Jiang and Hank Walker (*Texas A&M University*)
20: Explore the Limits to Reduce Test Power
Shaochong Lei (Xian JiaoTong Univ.), **Z. Jiang, and D. M. H. Walker (***Texas A&M Univ.***)**

Coffee Break- 10:20am - 10:40am

10:40am - 12:pm
Session 3: Signal and Power Integrity
*Chair - **Suriyaprakash Natarajan** (Intel)*

20: Identification of IR-drop Hot-spots in Defective Power Distribution Network Using TDF ATPG
Junxia Ma, Jeremy Lee, Mohammad Tehranipoor *(Univ. Of Connecticut)***, Xiaoqing Wen** *(KIT Univ.)***, Al Crouch** *(Asset-Intertech)*
30: Timing closure: Requirements for Variation Aware Design (*Invited Talk*)
Ayhan Mutlu (*Extreme DA*)
30: Plugging Some Limitations of Structural Testing (*Invited Talk*)
Sreejit Chakrabarty (*LSI Logic*)

Lunch - 12:0 pm - 1:00pm

1:00pm - 2:20pm
Session 4: Yield and Data Analysis
*Chair – **Anuja Banerjee** (nVidia)*

30: Collecting Realistic Data for Parametric Yield *(invited talk)*
Amit Majumdar (*AMD*)
30: Linking Design and Test for Yield Learning through STDF (*Invited Talk*)
Ajay Koche (*Verigy***)**
20: A Flexible Scan Architecture to Enable Detection of Stuck-at and Small Delay Defects of a Multi-core Microprocessor Design
Talal Jaber and David Wu *(Intel)*

Short Break- 2:20pm - 2:30pm

2:30pm - 4:00 pm ***- Panel Discussion***
Challenges in Test Data Collection & Analysis

Organizers:
Adit Singh *(Auburn Univ.)*
Mohammad Tehranipoor *(Univ. of Connecticut)*

Panelists:
Keith Arnold (Pintail)
Bruce Cory (Nvidia)
Mike Laisne (Qualcomm)
Jay Orbon (Verigy)
Al Crouch (Asset-Intertech)